

FIG. 1

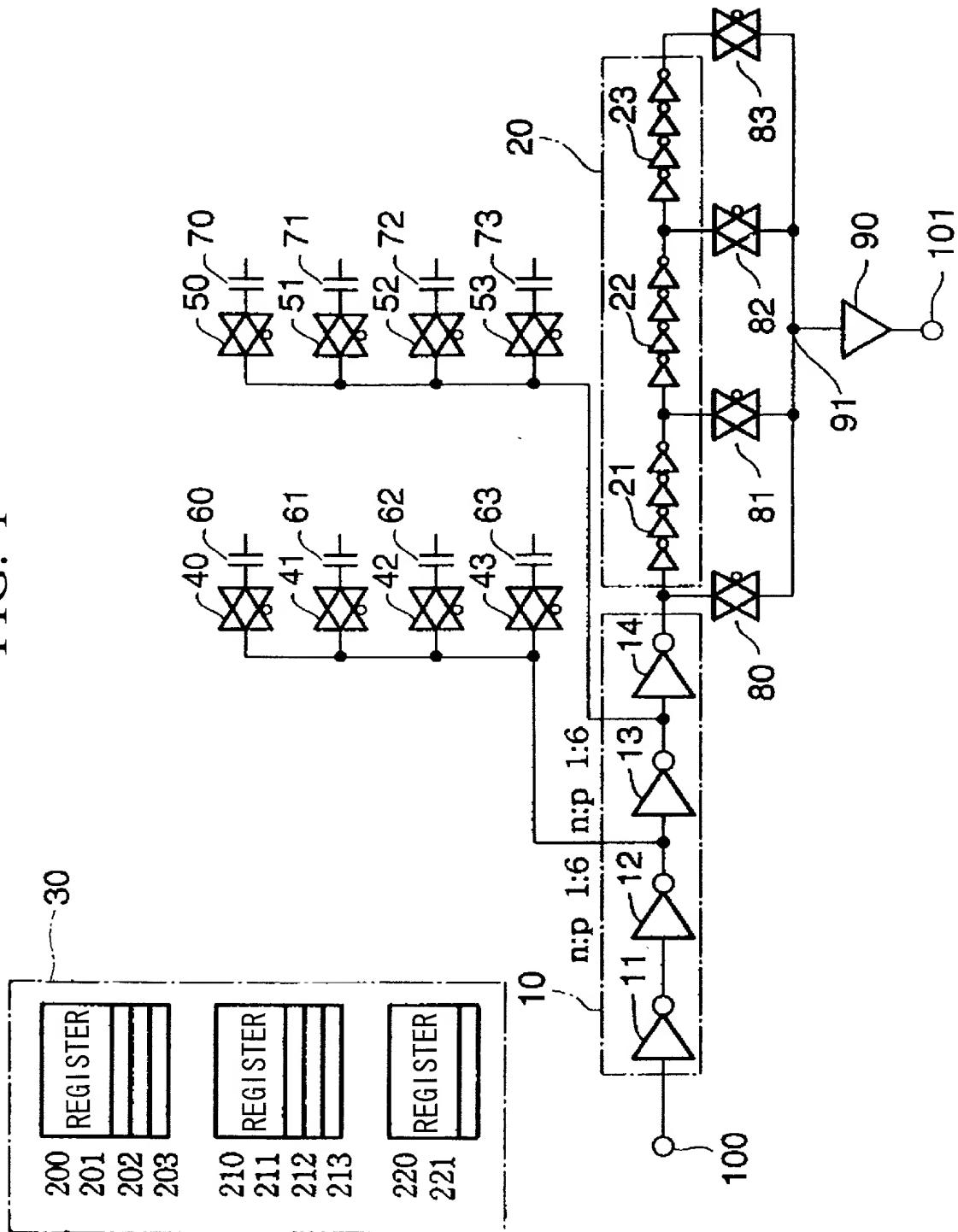


FIG. 2

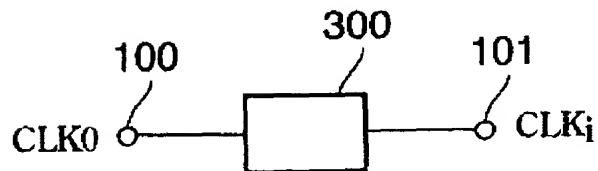


FIG. 4

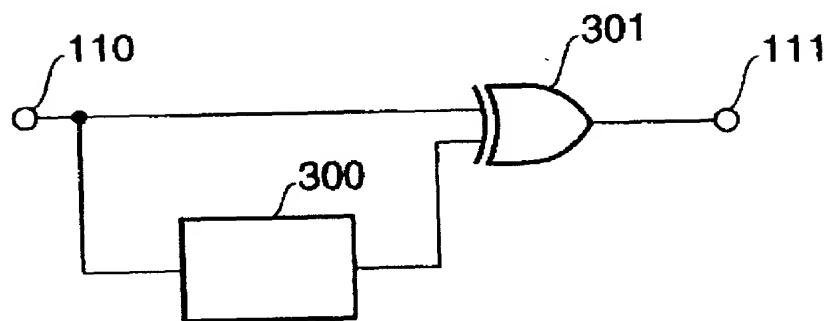
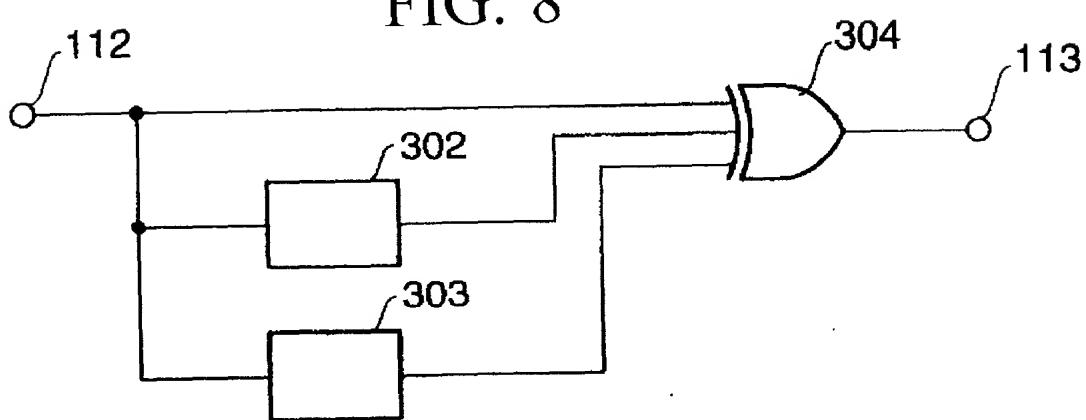
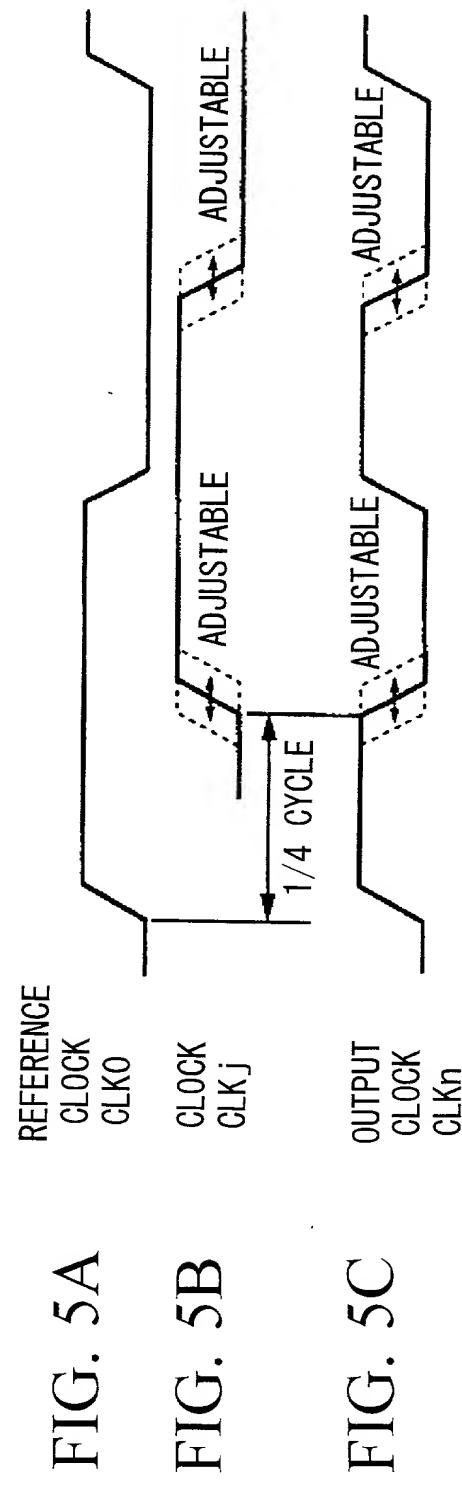
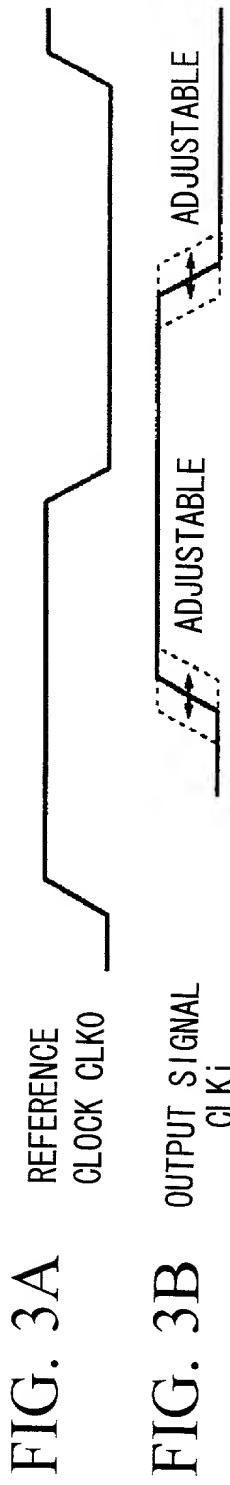


FIG. 8





Title: DELAY ADJUSTMENT CIRCUIT
AND A CLOCK GENERATING CIRCUIT
USING THE SAME
Inventor(s): Atsushi YOSHIKAWA, et al
Atty. Docket No. 088941/0184
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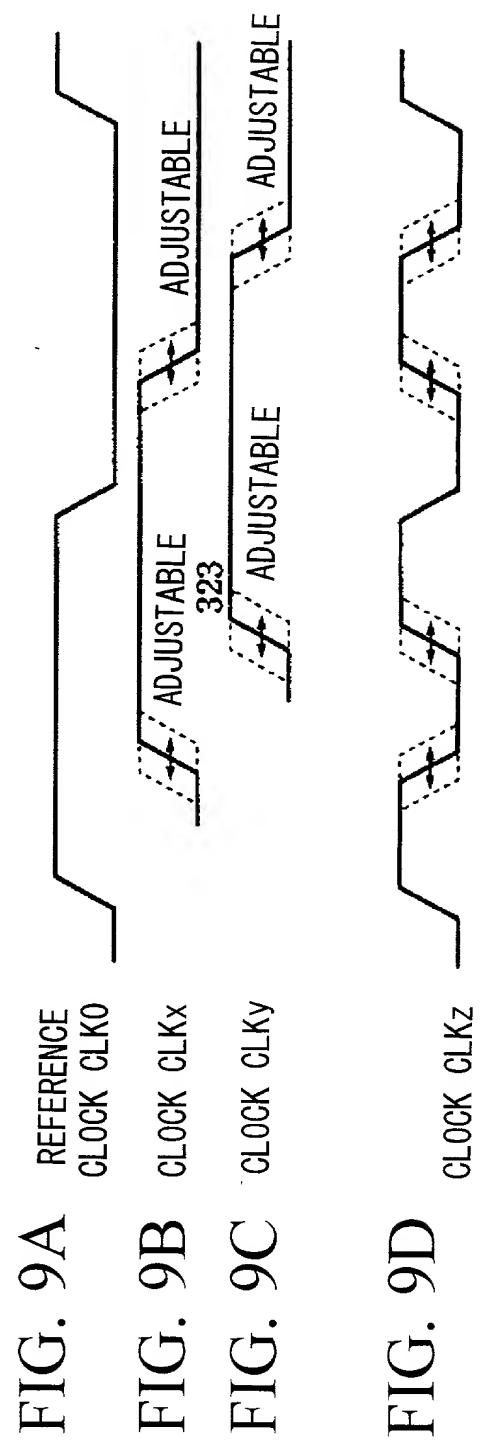
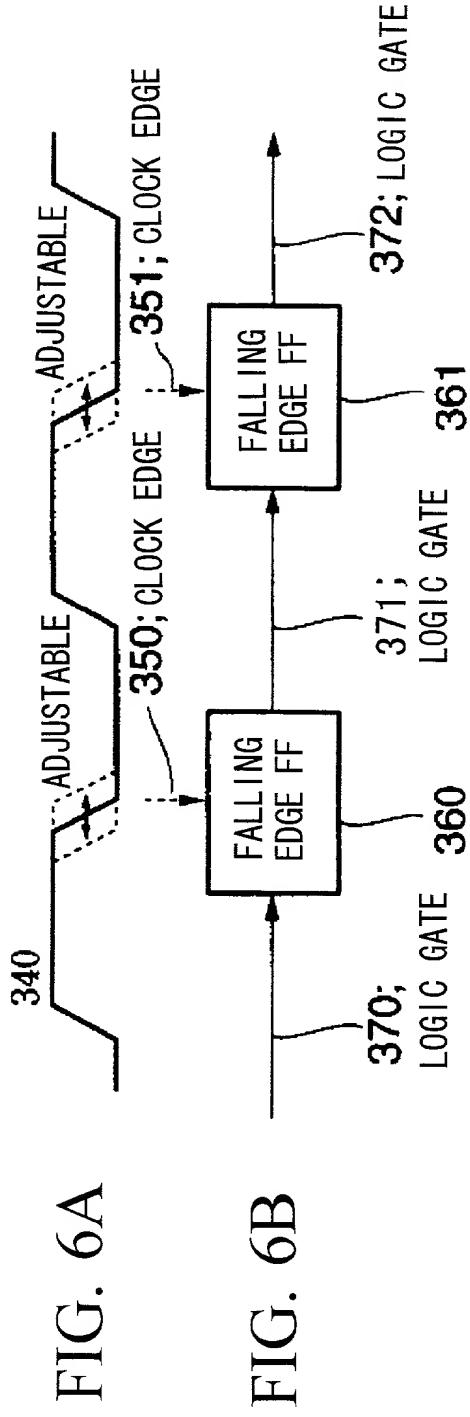


FIG. 7

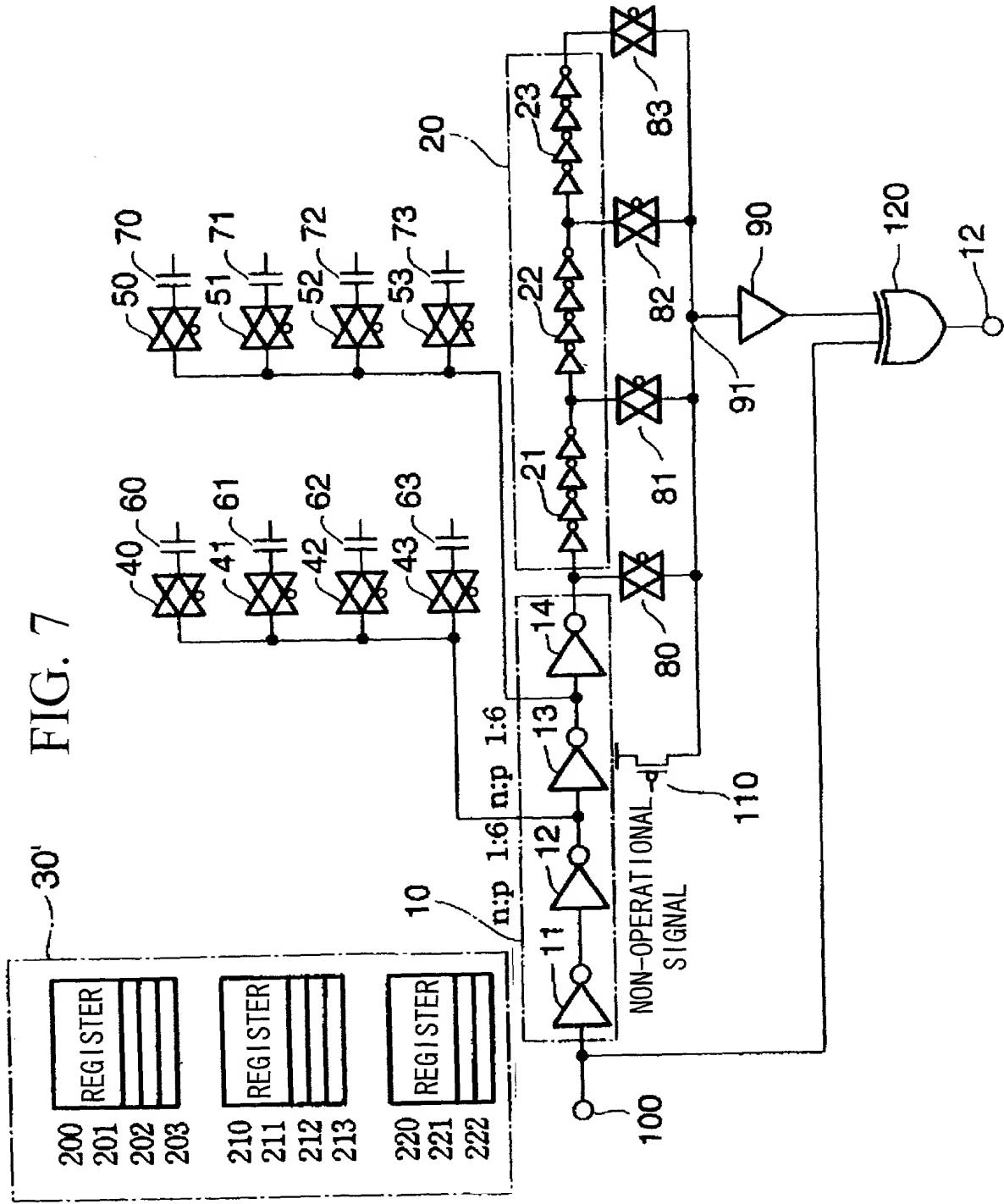


FIG. 10
400; CLOCK GENERATING CIRCUIT

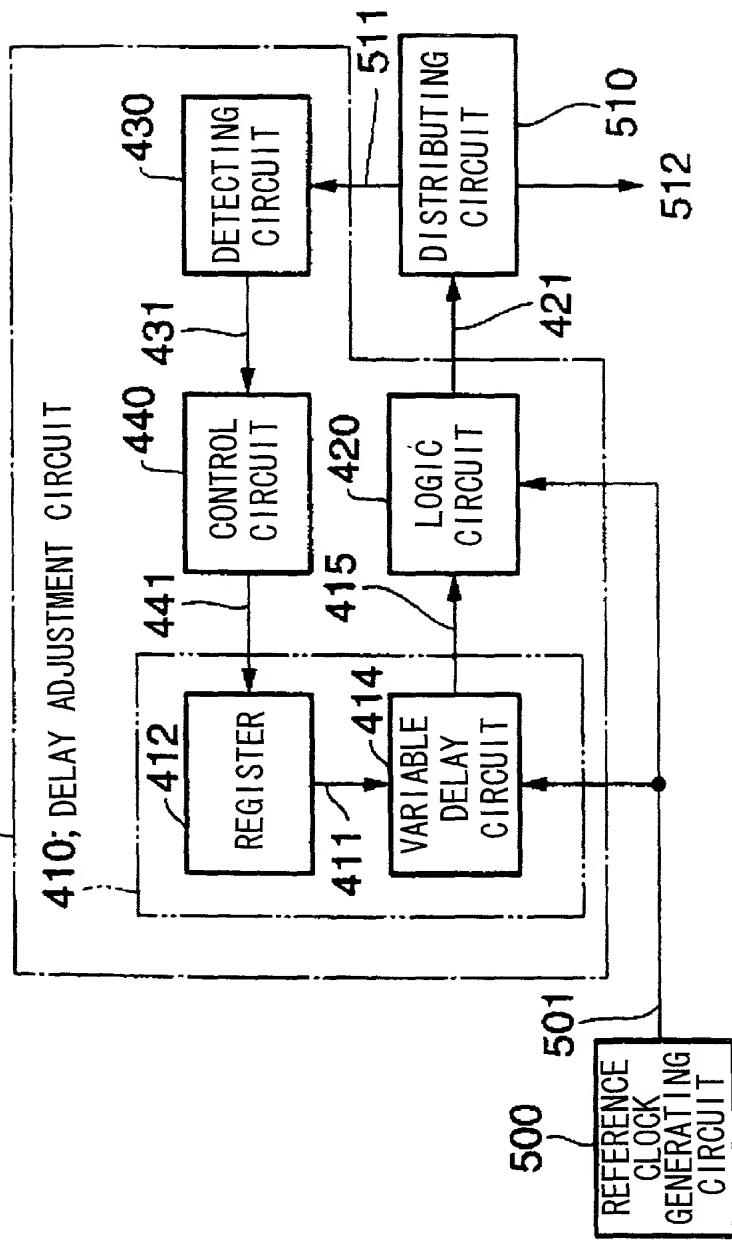


FIG. 11

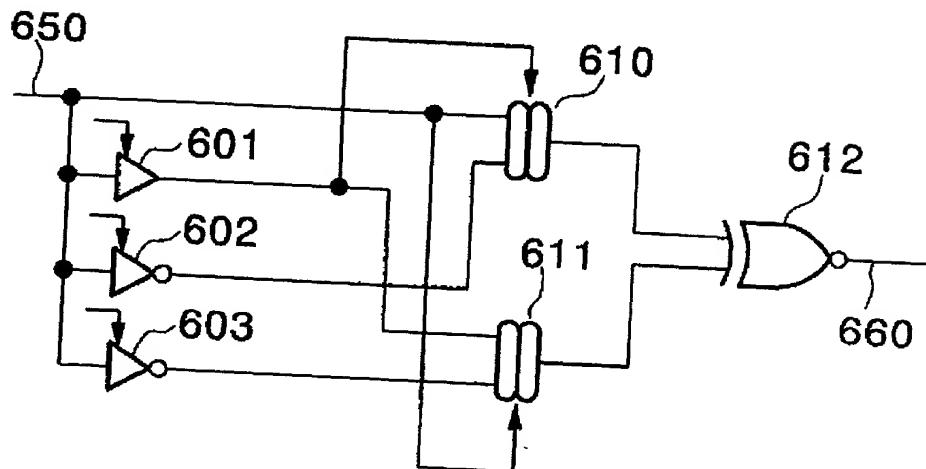


FIG. 13

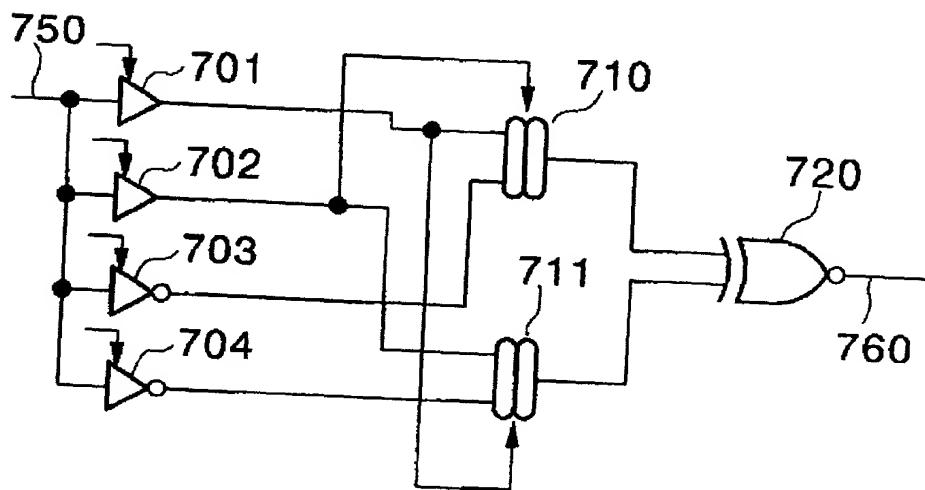


FIG. 12A INPUT SIGNAL 650

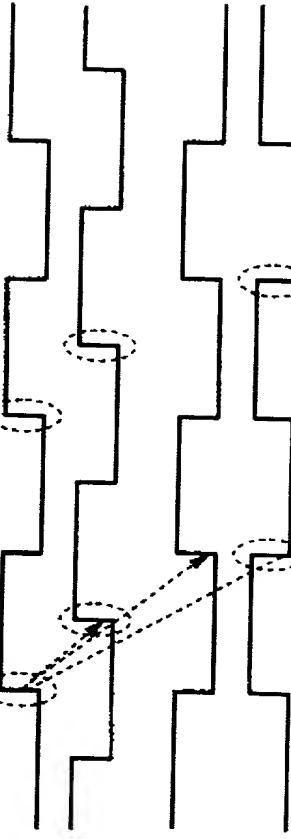


FIG. 12B OUTPUT SIGNAL OF 601

FIG. 12C 2/4 CYCLE DELAYED SIGNAL OF 650

FIG. 12D OUTPUT SIGNAL OF 602
3/4 CYCLE DELAYED

FIG. 12E SIGNAL OF INPUT SIGNAL 650

FIG. 12F OUTPUT SIGNAL OF 603

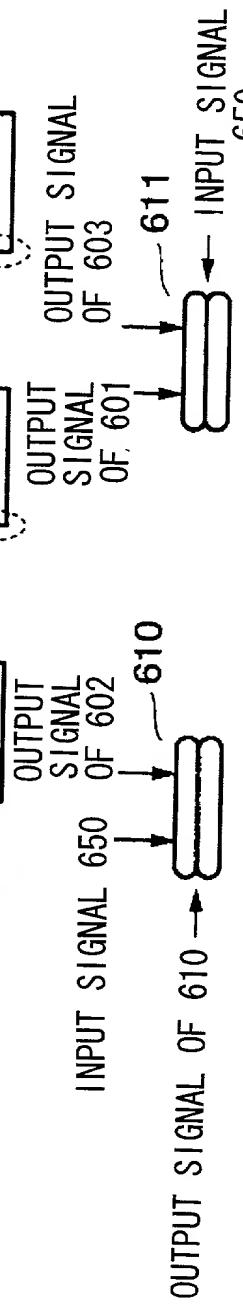


FIG. 12G OUTPUT SIGNAL OF 601

FIG. 12H OUTPUT SIGNAL OF 611



FIG. 12I OUTPUT SIGNAL 660



FIG. 14

